Design Considerations for a Voltage-Boosting DC-AC Modular Multilevel Converter

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1. INTRODUCTION

The Modular Multilevel Converter (M2C) is a relatively recent addition to the family of multilevel power converters [l]. This converter family utilizes many interconnected submodules to form a collective converter. It is often used when performance requirements exceed what conventional 2- level power converters can offer, whether in terms of switching frequency, individual semiconductor voltage blocking capability, EMI, or other metrics. Throughout its short history the M2C has been positioned as having very attractive attributes in HVDC applications [2] because the modular and multilevel nature is conducive to extremely high voltages, the series interleaving of low switching frequencies which enables very high effective ripple frequencies to minimize line filters, high phase current controllability even during fault events, and so on. The M2C has also been proposed for use in much lower voltage, lower power applications as a converter on a silicon chip [3], which takes advantage of extremely high switching frequencies with minimal filtering.

In HVDC applications, the functional need for boosting of low ac voltages to higher de voltages permits the use of the half bridge submodule in place of the full bridge submodule [4], effectively eliminating half of the semiconductor components [5], which reduces converter cost and improves converter efficiency. If the ac voltage and the de voltage are of comparable magnitude, the use of full bridge submodule realization of the M2C is required. On the other hand, applications that call for boosting low de voltages to higher ac voltages (for instance, solar PV inverters) using M2C conversion approaches have not been studied extensively in the literature [6, 7]. This paper presents the operation of M2C to such DC to AC voltage boosting applications.

The use of an alternative semi-full bridge submodule suitable for conversion between low de and high ac voltages to complement the half bridge and full bridge submodules is developed. The work is further differentiated from other M2C investigations by specifically addressing PWM-based conversion, as opposed to staircase modulation, which is more typical in HVDC applications.

The general M2C-based DC-AC topology and submodule choices are introduced in Section II, outlining the operational limits of the submodules. Section III discusses the concept of the "per unit" submodule converter using averaged modeling. Section IV introduces a closed loop control methodology, which is used in Section V to facilitate a dynamic phasor circuit model. An analysis of the system eigenvalues is presented in Section VI with extensions to higher numbers of "per unit" submodules. Finally, the models are validated using simulations and experimental results in Section VII.

II.. CONVERTER TOPOLOGY

A generalized M2C-based DC-AC power converter is shown in Fig. 1. The converter contains three phase legs, where each phase leg comprises two current-stiff arms. Each arm, in turn, comprises *ns* series-connected submodules (SMs) and arm inductors L_{SM}

A definition is made wherein the neutral points of the de and ac sides are set as the mean of both the de and ac sources, respectively. Thus, the two nodes may be considered to nominally be at equipotential whether or not a galvanic connection exists. In this way, the arm voltages and currents are determined by relatively few circuit components and the remainder of the converter network can be neglected.

The topological construction of an SM is very flexible because it only needs to behave as a controlled voltage source with some amount of internal energy storage. The necessary

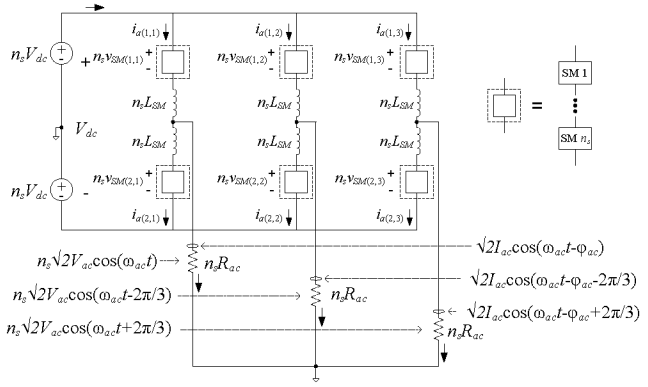

Fig. 1. M2C-based DC-AC 3-phase power converter.

terminal characteristics of the SM are determined by its surrounding converter terminal characteristics. For example, an arbitrary arm current and voltage are represented as

$$i_a(t) = \frac{I_{dc}}{3} - \frac{I_{ac}}{\sqrt{2}}\cos\left(\omega_{ac}t - \varphi_{ac}\right) \tag{1}$$

$$n_s v_{SM}(t) = n_s V_{dc} - \sqrt{2} n_s V_{ac}\cos\left(\omega_{ac}t\right), \tag{2}$$

where the inductor is assumed small, the inductor voltage is neglected, all ac quantities are rms values, and ϕ_{ac} is the power factor angle. The actual construction of a SM is then determined by the unidirectional/bidirectional nature of $i_a(t)$ and $nv_{SM}(t)$, which is in turn determined by the relative magnitudes of V_{dc}, V_{ac}, I_{dc} and I_{ac}.

Three basic types of SMs exist, which are shown in Fig. 2 and are classified according to their terminal characteristics: Unidirectional Voltage (UV) vs. Bidirectional Voltage (BV) and Unidirectional Current (UC) vs. Bidirectional Current (BC). The half bridge (HB) and full bridge (FB) are very well-known topologies, and have UVBC and BVBC characteristics, respectively. The HB is generally the more desirable of the two due to a lower parts count and therefore lower cost.

The third SM is the semi-full bridge (SFB), which contains the same number of components as the half bridge, but arranged similar to the full bridge [8]. It is a complement to the half bridge, having a BVUC characteristic. It is particularly attractive because it is immune to shoot-through faults, making it more robust than the HB or FB SMs.

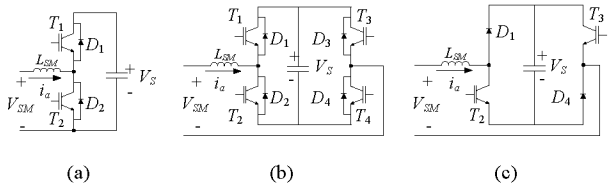

Fig. 2. Types of submodules: (a) half bridge (UVBC), (b) full bridge (BVBC), and (c) semi-full bridge (BVUC).

Considering steady-state converter operation, the SFB is suitable for high I_{dc} and low I_{ac}, which makes it the ideal candidate for voltage-boosting DC→AC power converters. This is in stark contrast to the HB, which is found in HVDC converters where high I_{ac} and low I_{dc} are found.

Classifying the SMs is facilitated using the voltage transfer ratio,

$$k_{tr} = \frac{V_{dc}}{V_{ac}}, \tag{3}$$

where V_{dc} represents the line-neutral voltage at the dc port, and V_{ac} represents the rms line-neutral voltage at the ac port. This ratio is useful because the limitations of each SM – unidirectional voltage or unidirectional current – relate to specific values of k_{tr}. For example, the HB SM is limited to unidirectional voltage. Starting with (2) and applying (3):

$$V_{dc} - \sqrt{2}V_{ac}\cos\left(\omega_{ac}t\right) \geq 0 \tag{4}$$

yields

$$k_{tr} \geq \sqrt{2} \tag{5}$$

On the other hand, the SFB SM is limited to unidirectional current. To directly relate k_{tr} to I_{dc} and I_{ac}, the power converter is assumed to be 100% efficient, hence

$$V_{dc}I_{dc} = \frac{3}{2}V_{ac}I_{ac}\cos\left(\phi_{ac}\right) \tag{6}$$

and therefore

$$k_{tr} = \frac{3I_{ac}}{2I_{dc}}\cos\left(\phi_{ac}\right). \tag{7}$$

For the condition of

$$\frac{I_{dc}}{3} - \frac{I_{ac}}{2}\cos\left(\omega_{ac}t - \phi_{ac}\right) \geq 0 \tag{8}$$

the corresponding relationship is

$$k_{tr} \leq \frac{1}{\sqrt{2}}\cos\left(\phi_{ac}\right). \tag{9}$$

These limits on k_{tr} are illustrated in Fig. 3 over varying power factors.

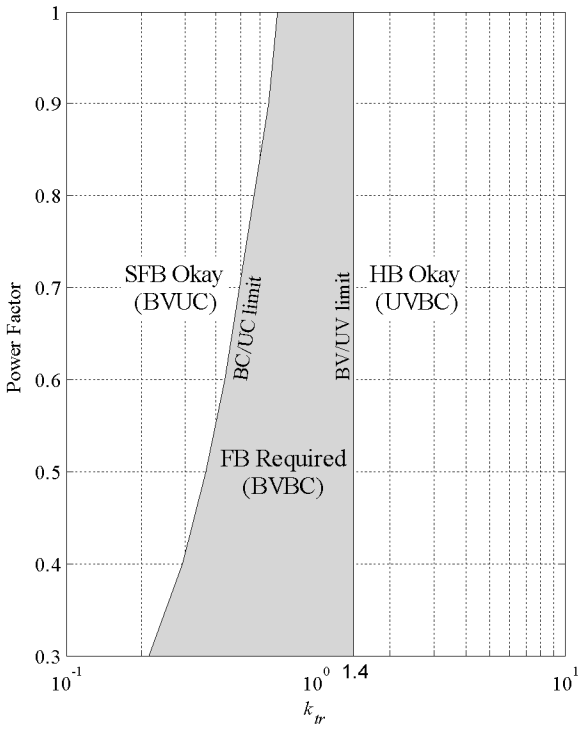

Fig. 3. Suitability of SM types as a function of voltage transfer ratio k_{tr} and power factor.

III. "PER UNIT" SUBMODULE AVERAGED MODEL

Deep insight into the converter steady-state behavior and dynamics may be gained by applying an averaged circuit model as developed in [9], including a nominal load resistor R_S on each SM to represent power loss and/or local SM loading. Fig. 4 illustrates such a model, which considers only a single SM; the model will be scaled up in Section V. Neglecting the inductor voltage, the SM terminal voltage is equal to the product of the SM duty ratio d_{SM} and the effective capacitor voltage v_S. Likewise, the SM capacitor current is equal to the product of d_{SM} and the arm current i_a (less the resistive loss).

Two assumptions are established to simplify analysis. First, the capacitance C_S is assumed large and thus v_S is essentially dc. Second, the total arm inductance is very small so its voltage is neglected. Using the averaged model within the converter of Fig. 3, the steady state solution for the duty ratio is therefore

$$d_{SM}(t) = \frac{V_{dc}}{v_S} - \frac{\sqrt{2}V_{ac}}{v_S}\cos(\omega_{ac}t), \tag{10}$$

which may also be expressed using (3) as

$$d_{SM}(t) = \frac{M}{k_{tr}+\sqrt{2}}\left(k_{tr} - \sqrt{2}\cos(\omega_{ac}t)\right), \tag{11}$$

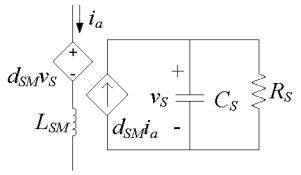

Fig. 4. Averaged model of single SM.

where the *modulation index* M is defined as

$$M = \frac{V_{dc}}{v_S}\left(1 + \frac{\sqrt{2}}{k_{tr}}\right) \tag{12}$$

and may have values between 0 and 1.

A. Capacitor design equations

With the above definitions, the capacitor current is expressed as

$$i_{Cs}(t) = C_S\frac{dv_S}{dt} = d_{SM}(t)i_a(t) - \frac{v_S}{R_S}, \tag{13}$$

which may be rewritten in terms of k_{tr}, M and I_{dc}:

$$i_{Cs}(t) = \frac{M(I_{dc}/3)}{k_{tr}+\sqrt{2}}\left(\sqrt{2}\left(k_{tr}^2 - 1\right)\cos(\omega_{ac}t) - k_{tr}\cos(2\omega_{ac}t)\right) - \frac{v_S}{R_S} \tag{14}$$

Note that this current model includes the minimum frequency content, i.e. ω_{ac} and $2\omega_{ac}$, which results from the ω_{ac} product term in (13). These definitions then give rise to the rms capacitor current,

$$i_{Cs,rms} = \frac{M(I_{dc}/3)}{k_{tr}+\sqrt{2}}\sqrt{k_{tr}^4 - \frac{3}{2}k_{tr}^2 + 1} \tag{15}$$

B. Choice of L_{SM}

One very attractive characteristic of the M2C is its ability to tolerate very small values of L_{SM}. This is enabled by the use of many series-connected SMs, which allow series interleaving of the PWM switching, effectively multiplying the switching frequency F_S by n_s [6]. In fact, in some of the literature, the presence of L_{SM} is not even recognized formally, and implicitly assumed to be the parasitic inductances of the circuit paths.

With small values of L_{SM}, open loop converter operation can pose challenges because additional, unintended dynamics can appear due to the nonlinear product terms exciting converter harmonics and/or resonances. For example, Fig. 5 shows simulation waveforms of an averaged actual arm current alongside its intended trajectory, where currents at higher order frequencies actually dominate the waveform. The additional

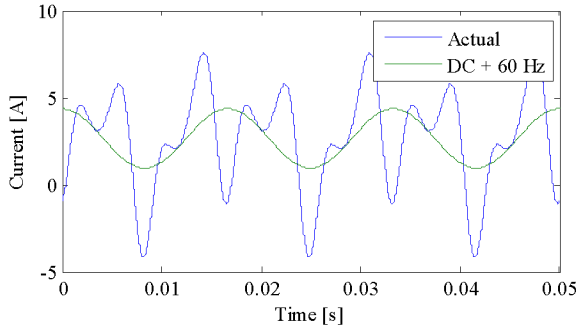

Fig. 5. Simulations showing effect of open loop duty ratio control on arm current with small L_{SM}, compared to intended trajectory of purely dc + 60 Hz.

frequency content increases converter losses and, in the case of even harmonics appearing in single-phase dc-ac converter arms, can inject these significant currents into the dc port. These additional frequency components within the arm currents are therefore extremely undesirable and a mitigation method is warranted.

IV. SHOTS Controller

Closed loop arm current control is an effective way to mitigate unwanted arm current components [10]. Even though the duty ratio may consist entirely of dc and ω_{ac} components, these "higher order terms" are the result of the nonlinear terms in (10) and (13), producing additional frequencies within v_S and i_a. Using a scalar methodology with proportional gain as presented in [9,10], a Scalar Higher Order Term Suppression (SHOTS) controller is proposed as shown in Fig. 6.

To facilitate modularity of the arm model, the ac load R_{ac} is considered independently across arms within a phase leg. Therefore the effective resistance is $2R_{ac}$. Balanced operation across arms is also assumed, leading to current sources $i_1 = I_{ac}/2$ and $i_2 = I_{dc}/3$ to prevent ac current from flowing through V_{dc} and vice-versa.

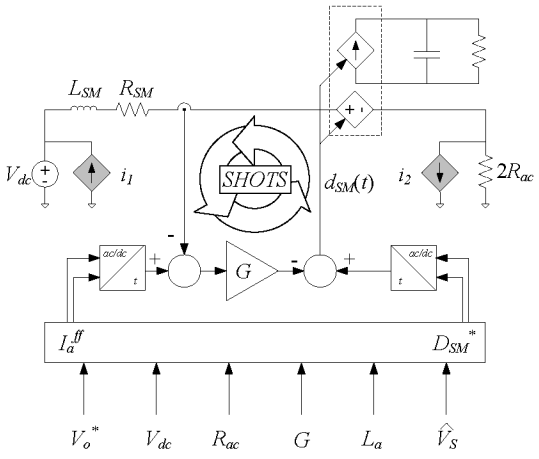

Fig. 6. Structure of Scalar Higher Order Term Suppression (SHOTS) controller.

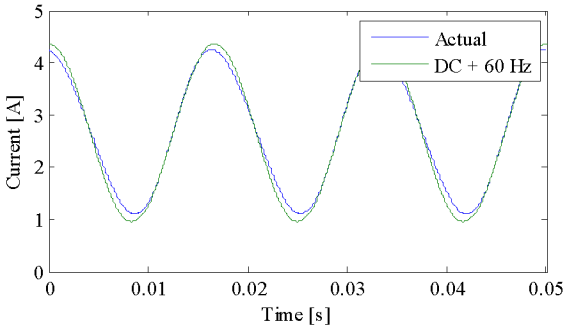

Fig. 7. Simulations showing effect of SHOTS control on arm current with small L_{SM}. $G = 0.05$, demonstrating significant reduction in harmonic content.

The effect of implementing SHOTS control on one M2C arm current is shown in Fig. 7, which demonstrates a significant reduction in arm current harmonics as compared to Fig. 5. The quantified reduction in rms arm current is presented in TABLE I.

TABLE I. Reduction of RMS Current using SHOTS Controller

	Analytical Model	**Simulation**	
		***G* = 0**	***G* = 0.05**
$i_{a,rms}$	2.8 A	3.9 A	2.9 A

V. Dynamic Phasor Model

A. Per unit converter

The presence of ac waveforms within the M2C motivates the use of phasor modeling to describe behavior and understand inner dynamics. Previous M2C dynamic models used scalar approaches [11], which are only able to capture a portion of the converter dynamics, e.g. fundamental ac frequency behavior is not captured.

A dynamic phasor model of an M2C using a "per unit" SM is used, which is based on d, q and dc components as described in [12]. The model represents the terminal ac voltage in the well-known d-q reference coordinates, wherein the ac time varying quantities are represented by complex phasors having real (d) and imaginary (q) quantities. This model uses ac coordinates described by the phasor diagram of Fig. 8. The dynamic model equations are described in (16)-(19). Since the inductor current has dc as well as ac quantities superimposed upon each other, it is resolved into d, q and dc quantities. The dynamic equations of the inductor current may be resolved into 3 relationships (16)-(18). On the other hand, the submodule energy storage capacitor voltage is where the interaction between the ac variables and the dc variables take place, as determined by the d-component of the duty ratio, q-component of the duty ratio, and the dc component of the duty ratio, as described in (19).

$$L_{SM}\frac{dI_{a,dc}}{dt} = V_{dc} - R_{SM}I_{a,dc} - D_{SM,dc}V_S \tag{16}$$

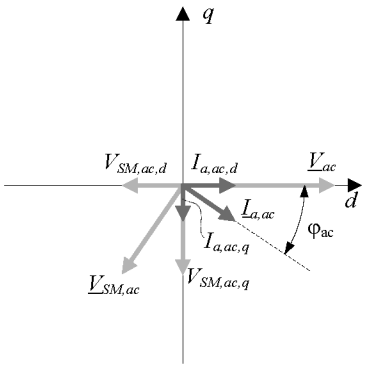

Fig. 8. Phasor diagram of the ac quantities of the M2C dynamic phasor model.

$$L_{SM}\frac{dI_{a,ac,d}}{dt}=\omega_{ac}L_{SM}I_{a,ac,q}-\left(R_{SM}+2R_{ac}\right)I_{a,ac,d}-D_{SM,ac,d}V_S \tag{17}$$

$$L_{SM}\frac{dI_{a,ac,q}}{dt}=-\omega_{ac}L_{SM}I_{a,ac,d}-\left(R_{SM}+2R_{ac}\right)I_{a,ac,q}-D_{SM,ac,q}V_S \tag{18}$$

$$C_S\frac{dV_S}{dt}=D_{SM,dc}I_{a,dc}+D_{SM,ac,q}I_{a,ac,q}+D_{SM,ac,d}I_{a,ac,d}-\frac{V_S}{R_S} \tag{19}$$

B. *Scale up using n_s*

Using the concept of the "per unit" SM, additional SMs may be connected in series within each arm, each with identical circuit parameters and therefore each adding an equal "per unit" value of power throughput. When each arm comprises n_s series-connected submodules, we may assume the nominal d-q-dc components of duty ratio across all the submodules. Because each SM has its own inductor L_{SM} with series resistance R_{SM}, and energy storage capacitor C_S, the total arm inductance is n_sL_{SM}, the total arm resistance is n_sR_{SM}, and the total effective capacitance is C_S/n_s. Furthermore, local resistance R_s at the energy storage bus of each submodules may be assumed to be identical to those of the per unit converter. A diagram of the arm circuit when using n_s submodules, SHOTS controller and the dynamic vector circuit model is shown in Fig. 9.

Under these assumptions, the dynamic model expressed in (16)-(19) may be readily extended to form equations (20)-(22) for the inductor current and (23) for the i^{th} capacitor voltage, where i may take values between 1 and n_s.

$$n_sL_{SM}\frac{dI_{a,dc}}{dt}=n_sV_{dc}-n_sR_{SM}I_{a,dc}-D_{SM,dc}\sum_{i=1}^{n_s}V_{S,i} \tag{20}$$

$$n_sL_{SM}\frac{dI_{a,ac,d}}{dt}=\omega_{ac}n_sL_{SM}I_{a,ac,q}-\left(n_sR_{SM}+2n_sR_{ac}\right)I_{a,ac,d}-D_{SM,ac,d}\sum_{i=1}^{n_s}V_{S,i} \tag{21}$$

$$n_sL_{SM}\frac{dI_{a,ac,q}}{dt}=-\omega_{ac}n_sL_{SM}I_{a,ac,d}-\left(n_sR_{SM}+2n_sR_{ac}\right)I_{a,ac,q}-D_{SM,ac,q}\sum_{i=1}^{n_s}V_{S,i} \tag{22}$$

$$C_S\frac{dV_{S,i}}{dt}=D_{SM,dc}I_{a,dc}+D_{SM,ac,q}I_{a,ac,q}+D_{SM,ac,d}I_{a,ac,d}-\frac{V_{S,i}}{R_S} \tag{23}$$

VI. Eigenvalue Analysis

The relationships (20)-(23) form the dynamic equations that determine the converter operation, and can be used to determine the steady state solution by setting the derivatives of the state variables to zero, and the small signal dynamics of the converter by evaluating the Jacobian of the dynamic system at the steady state operating point.

For instance, when considering a very well-regulated system, the steady state solutions of the per-unit converter may be determined as (24)-(27).

$$D_{SM,dc}=\frac{V_{dc}-R_{SM}I_{a,dc}}{V_S} \tag{24}$$

$$D_{SM,ac,d}=\frac{\omega_{ac}L_{SM}I_{a,ac,q}}{V_S}-\frac{\left(R_{SM}+2R_{ac}\right)I_{a,ac,d}}{V_S} \tag{25}$$

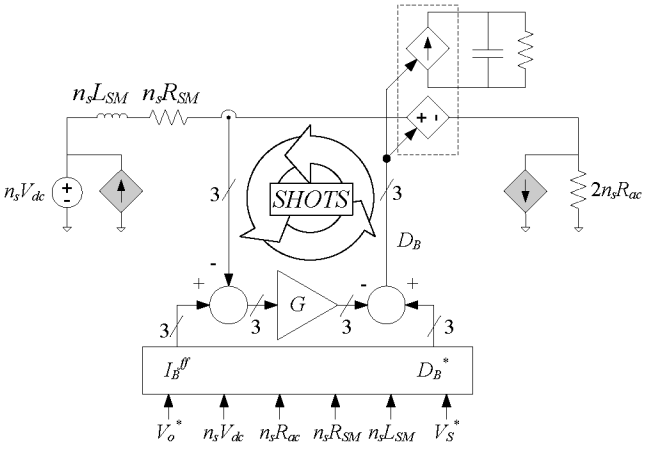

Fig. 9. Structure of Scalar Higher Order Term Suppression (SHOTS) controller when integrated into converter using d-q-dc dynamic vector model.

$$D_{SM,ac,q} = \frac{-\omega_{ac} L_{SM} I_{a,ac,d}}{V_S} - \frac{\left(R_{SM} + 2R_{ac}\right) I_{a,ac,q}}{V_S} \quad (26)$$

$$I_{a,dc} = \frac{V_{dc}}{2R_{SM}} - \sqrt{\frac{V_{dc}^2}{4R_{SM}} - \left(1 + \frac{2R_{ac}}{R_{SM}}\right)\left(I_{a,ac,d}{}^2 + I_{a,ac,q}{}^2 + \frac{V_S^2}{R_S R_{SM}}\right)} \quad (27)$$

The steady state solution of the n_s-submodule converter in terms of the branch inductor current d-q-dc components and the submodule dc capacitor voltage are identical to those of the per unit converter solution, if the duty ratio of d-q-dc components of all the submodules, and the local load resistance R_s at the energy storage bus of all the submodules are identical to those of the per unit converter.

It can be shown that an n_s-submodule converter has n_s+3 eigenvalues. Of these eigenvalues, (n_s-1) are caused by the $R_S C_S$ dynamics at the dc bus of each SM. One of the remaining pairs of eigenvalues is an underdamped complex pair caused by the power frequency of excitation, ω_{ac}. The remaining pair of eigenvalues is highly damped and is produced by the resonance of L_{SM} and C_S, modulated by $D_{SM,dc}$, where the damping is caused by proportional gain G. The eigenvalues can therefore be summarized as shown in TABLE II.

TABLE II. GENERALIZED EIGENVALUE LOCATIONS

Eigenvalue	Location
λ_1	$j\omega_{ac}$
λ_2	$-j\omega_{ac}$
$\lambda_3\,\lambda_4$	$D_{SM,dc}{}^2 / L_{SM} C_S$
$\lambda_{5\ldots ns}$	$1/R_S C_S$

In other words, adding "per unit" submodules to a given converter, where all submodules share the same circuit parameters and operating points, only adds one eigenvalue per submodule, located at $1/R_S C_S$. No other eigenvalues are affected.

VII. TESTBED VERIFICATION

Verification of the analytical modeling presented in this work is provided through experimental and simulation platforms. This section describes each platform in detail, then uses the platforms to verify the analytical model.

A. Experimental prototype

A 15 V_{dc} → 25 $V_{ac,rms}$ laboratory-scale prototype converter with n_s = 3 submodules per arm and single phase ac output was constructed per the schematic in Fig. 10. The actual converter was built from the submodule boards of Fig. 12, which were then assembled into the upper portion of the rack in Fig. 11, and a Converter Controller circuit board located below. A photo of one submodule board is shown in Fig. 12. Data communications between the submodules and Converter Controller was provided by CAN, and an isolated high-speed synchronization pulse signal between submodules facilitates PWM clock synchronization and interleaving.

Each submodule board contains a power bridge with energy storage capacitors and inductor, in addition to its own intelligence, comprising a Microchip dsPIC33FJ64GS606 microcontroller, sensing circuitry, fault protection, communications, and housekeeping power supplies. These supplies provide constant-voltage power to the various electrical loads, deriving their power from the energy storage capacitor directly, and therefore do not require external power supplies for submodule control.

The Converter Controller board provides a centralized communications platform to interface the converter as a whole with a PC via serial connection. The heart of this controller is a Texas Instruments F28M35 Concerto dual core MCU, which provides ample computational throughput to maintain communications across submodules, and leaves room for future expansion into centralized control methodologies.

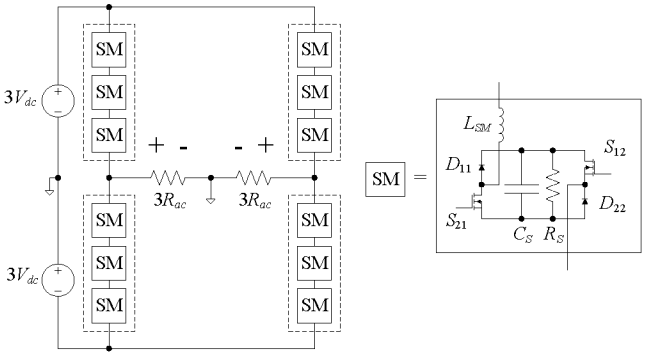

Fig. 10. Schematic of experimental n_s=3 lab-scale prototype converter using SFB submodules.

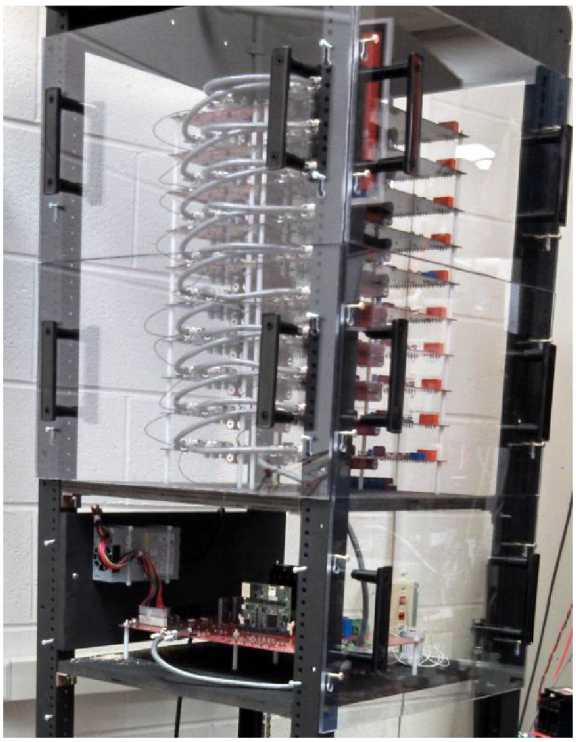

Fig. 11. Photograph of experimental n_s=3 lab-scale prototype converter.

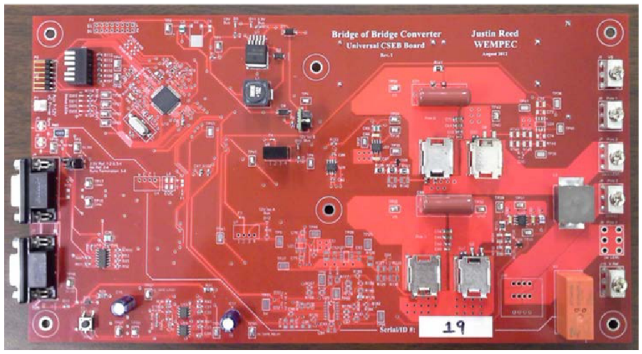

Fig. 12. Front of individual submodule circuit board. Energy storage capacitors are located on back of the board.

B. Simulation platform

Computer simulations were performed using MATLAB/Simulink R2011a with the PLECS Blockset 3.2.7 to model the actual circuit, including nonlinearities. The model encompasses a single phase leg with two arms feeding into one resistive ac load, R_{ac}. This is described in Fig. 13 and Fig. 14, with sample waveforms shown in Fig. 15.

C. Model verification

The analytical modeling validation is performed using one example operating point, given in TABLE III. The first form of validation comes by comparing the remainder of the operating point data of the analytical, simulation and experimental results, shown in TABLE IV, which all exhibit very good correlation.

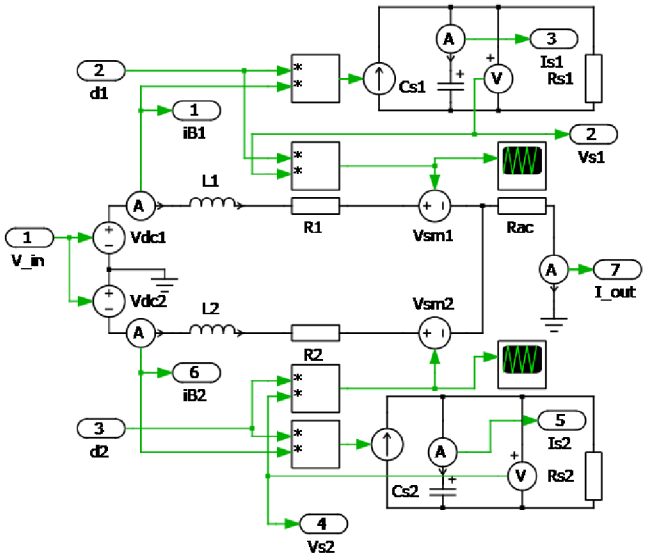

Fig. 13. PLECS circuit model of single phase leg with two arms.

TABLE III. MODEL VALIDATION OPERATING POINT

Parameter	Value	Parameter	Value
V_{dc}	14.1 V	C_S	5000 µF
$D_{SM,dc}$	15.9 %	R_S	750 Ω
L_{SM}	22 µF	n_s	3
R_{SM}	0.01 Ω	R_{ac}	2.7 Ω

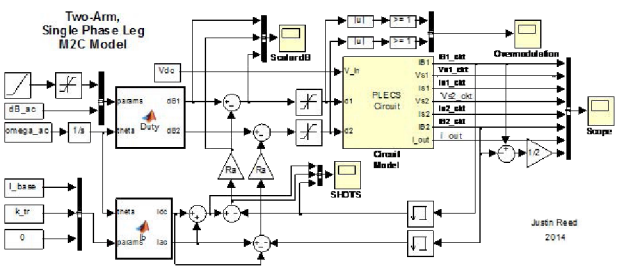

Fig. 14. Simulink model including PLECS circuit block.

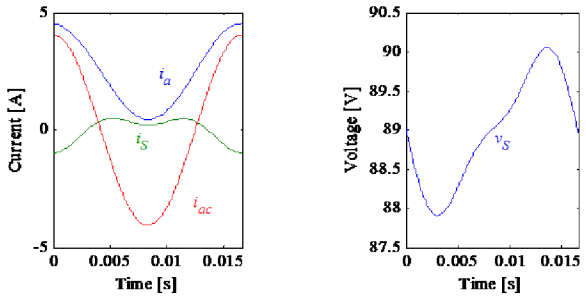

Fig. 15. Simulation waveforms using SHOTS (G=0.05), showing (a) arm current i_a, capacitor current i_S, and output current i_{ac}; (b) capacitor voltage v_S.

The second form of validation occurs using the capacitor current, with waveforms such as those in Fig. 16. When using G = 0.05 to attenuate unwanted frequencies, extremely good correlation of waveform shape results is demonstrated.

Verification of the BVUC bridge behavior using the experimental setup is shown at the high frequency switching level in Fig. 17, and at the low frequency ω_{ac} level in Fig. 18. Unidirectional arm current, bidirectional submodule voltage, and purely ac output current are observed.

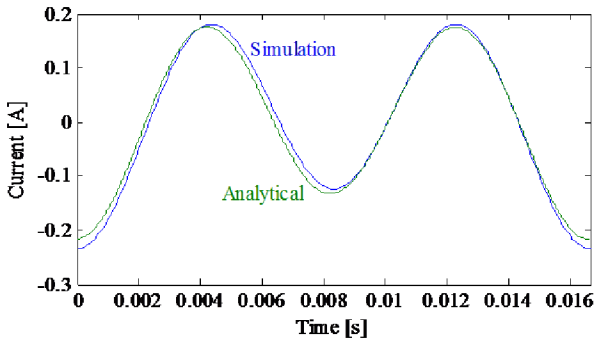

Fig. 16. Capacitor current waveform i_S, comparing simulations with analytical predictions. Simulations include G = 0.05 to maintain minimal harmonics. Operating Point Comparison

$D_{SM,ac}$	$V_{S,mod}$	$I_{a,ac,mod}$	$V_{S,sim}$	$I_{a,ac,sim}$	$V_{S,exp}$	$I_{a,ac,exp}$
0.060	29.68	0.326	31.8	0.328	29.9	0.33
0.120	29.68	0.652	31.8	0.651	29.6	0.57
0.180	29.68	0.979	31.7	0.980	28.9	0.94
0.240	29.68	1.305	31.5	1.303	28.0	1.23
0.300	29.68	1.631	31.3	1.631	27.2	1.55

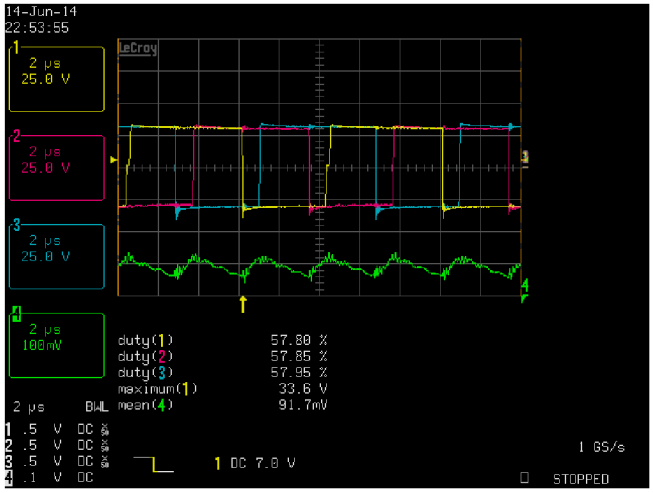

Fig. 17. Experimental waveforms showing 3 interleaved, bidirectional submodule terminal voltages with 100 kHz switching frequency, and arm current showing 300 kHz switching waveform with positive dc offset.

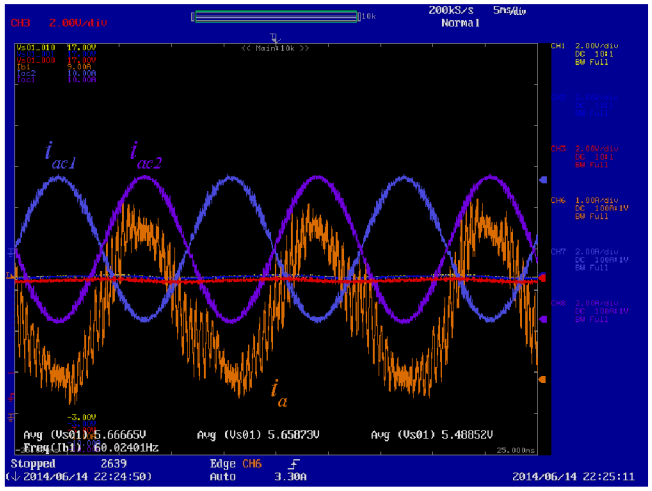

Fig. 18. Experimental waveforms showing two purely ac (bidirectional) output currents, one dc + ac unidirectional arm current, and 3 capacitor voltages of approximately 30V each.

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